

CLAIMS

What is claimed is:

- Sub B17
1. A metallization structure for a semiconductor device, comprising:
a substrate comprising a substantially planar upper surface;
a metal layer defining a pattern on a portion of the substrate upper surface;
a conducting layer overlying and substantially coextensive with the metal layer, said
metal layer and said conducting layer having substantially aligned sidewalls; and
metal spacers flanking the sidewalls of the conducting layer and metal layer.
 - 10 2. The metallization structure of claim 1, further comprising a dielectric layer
on the substrate upper surface and underlying the metal layer.
 - 15 3. The metallization structure of claim 2, wherein the dielectric layer is
silicon oxide or BPSG.
 4. The metallization structure of claim 1, wherein the metal layer is a first
metal layer comprising Ti, Ta, W, Co or Mo or alloys or compounds thereof, including
TaN or TiN.
 - 20 5. The metallization structure of claim 4, further including a second metal
layer disposed between the first metal layer and the substrate and comprising TiN, TiW,
WN, or TaN.
 - 25 6. The metallization structure of claim 5, wherein the first metal layer
comprises titanium or titanium nitride.
 7. The metallization structure of claim 1, wherein the metal layer is titanium
or titanium nitride.

8. The metallization structure of claim 1, wherein the conducting layer is selected from the group comprising aluminum and copper.

9. The metallization structure of claim 8, wherein the conducting layer is an aluminum-copper alloy.

10. The metallization structure of claim 1, wherein the metal spacers comprise at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

11. The metallization structure of claim 11, wherein the metal spacers are titanium or titanium nitride.

12. The metallization structure of claim 1, further comprising a dielectric layer on the conducting layer and having sidewalls aligned therewith, the metal spacers extending along the sidewalls of the dielectric layer. *with said sidewalls of the conducting layer*

13. The metallization structure of claim 12, wherein the dielectric layer comprises a low dielectric constant material.

14. The metallization structure of claim 13, wherein the dielectric layer is fluorine-doped silicon oxide.

15. The metallization structure of claim 1, wherein the metal layer and the metal spacers comprise the same metal.

16. A metallization structure for a semiconductor device, comprising:
a substrate having a metal layer disposed thereon;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer;
a metal spacer on the at least one sidewall of the aperture; and
a conductive layer substantially filling a remaining portion of the aperture.

5 17. The metallization structure of claim 16, wherein the metal layer comprises tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN.

10 18. The metallization structure of claim 17, wherein the metal layer is titanium or titanium nitride.

15 19. The metallization structure of claim 16, wherein the ~~at least one~~ metal spacer includes at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN.

20 20. The metallization structure of claim 19, wherein the ~~at least one~~ metal spacer is titanium or titanium nitride.

25 21. The metallization structure of claim 16, wherein the substrate comprises a dielectric layer underlying the metal layer.

22. The metallization structure of claim 21, wherein the dielectric ^{layer} underlying the metal layer is silicon oxide or BPSG.

23. The metallization structure of claim 16, wherein the metal layer and the ~~at least one~~ metal spacer comprise the same metal.

24. The metallization structure of claim 16, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

5 25. The metallization structure of claim 24, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

10 26. The metallization structure of claim 16, further comprising at least one upper metal layer on the conductive layer and comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

15 27. The metallization structure of claim 26, wherein the at least one upper metal layer comprises a plurality of upper metal layers.

28. The metallization structure of claim ²⁶16, wherein the at least one upper metal layer comprises titanium or titanium nitride.

20 29. A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal layer over the first dielectric layer;

forming a conducting layer over the metal layer;

forming a second dielectric layer over the conducting layer;

25 removing aligned portions of the second dielectric layer, ^{the} conducting layer, and ^{the at least one} metal

layer to form a multi-layer structure; and

forming metal spacers on sidewalls of the multi-layer structure.

30. The method of claim 29, wherein forming the first dielectric layer comprises forming a silicon oxide or BPSG layer.

31. The method of claim 29, further including forming the at least one metal layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

32. The method of claim 31, further including forming a second metal layer between the ^{at least one} first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

33. The method of claim 29, further including forming the at least one metal layer of titanium or titanium nitride.

34. The method of claim 29, wherein the at least one metal layer is a single metal layer and further comprising forming the single metal layer of titanium or titanium nitride.

35. The method of claim 29, further comprising forming the conducting layer from the group comprising aluminum and copper.

36. The method of claim 35, further including forming the conducting layer of an aluminum-copper alloy.

37. The method of claim 29, further including forming the metal spacers of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

38. The method of claim 37, further including forming the metal spacers of titanium or titanium nitride.

39. The method of claim 29, further comprising forming a dielectric layer on the conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal spacers to extend along the sidewalls of the dielectric layer. *of the conducting layer*

40. The method of claim 39, further comprising forming the dielectric layer of a low dielectric constant material.

41. The method of claim 40, further comprising forming the dielectric layer of a fluorine-doped silicon oxide.

42. The method of claim 29, further comprising forming the at least one metal layer and the metal spacers of the same metal.

43. The method of claim 29, further comprising forming the at least one metal layer by vapor deposition.

44. The method of claim 42, further comprising forming the at least one metal layer by CVD, PVD or PECVD.

45. The method of claim 29, further comprising forming the conducting layer by vapor deposition.

46. The method of claim 45, further comprising forming the conducting layer by CVD, PVD or PECVD.

47. The method of claim 29, further comprising forming the metal spacers by vapor deposition and directional etching.

48. The method of claim 47, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

5 49. The method of claim 29, wherein removing ^{the} aligned portions of the second dielectric layer, ^{the} conducting layer, and ^{the at least one} metal layer to form ^{the} a multi-layer structure is effected by patterning and etching the second dielectric layer, the conducting layer, and ^{the at least one} the metal layer.

10 50. The method of claim 29, further comprising forming the metal spacers by forming a metal spacer layer over the multi-layer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

15 51. The method of claim 50, further comprising forming the metal spacer layer over the multi-layer structure and first dielectric layer by a conformal deposition process.

52. The method of claim 51, wherein ^{the} portions of the metal ^{spacer} layer over the multi-layer structure and first dielectric layer are removed by etching.

20 53. The method of claim 29, further comprising:
removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto.

25 54. The method of claim 53, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal ^{spacers} ~~spaces~~ by etching.

55. A method for making a metallization structure comprising:
forming a substrate comprising at least one metal layer on ^a the surface thereof;
forming a dielectric layer over ^{the} at least one the metal layer;

forming an aperture having at least one sidewall through the dielectric layer to expose a surface of the at least one metal layer;
forming a metal spacer on the at least one sidewall of the aperture; and
forming a conductive layer in a remaining portion of the aperture.

5 56. The method of claim 55, further comprising forming the dielectric layer of silicon oxide.

10 57. The method of claim 55, further including forming the at least one metal layer of Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

15 58. The method of claim 57, wherein the at least one metal layer comprises a first metal layer, and further including forming a second metal layer between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

20 59. The method of claim 55, further including forming the at least one metal layer of titanium or titanium nitride.

60. The method of claim 55, further comprising forming the at least one metal layer by vapor deposition.

61. The method of claim 60, further comprising forming the at least one metal layer by CVD, PVD or PECVD.

25 62. The method of claim 55, further comprising forming the ~~conducting~~ ^{conductive} layer by vapor deposition.

63. The method of claim 62, further comprising forming the ~~conducting~~ ^{conductive} layer by CVD, PVD or PECVD.

64. The method of claim 55, further comprising forming the at least one metal layer and the metal spacer of the same metal.

5 65. The method of claim 55, further comprising forming the metal spacer by vapor deposition and directional etching.

66. The method of claim 55, further including forming the metal spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys or compounds thereof, including TaN or TiN.

10 67. The method of claim 66, further including forming the metal spacer of titanium or titanium nitride.

15 68. The method of claim 55, further comprising forming at least one upper metal layer on the conductive layer.

69. The method of claim 68, further comprising forming the at least one upper metal layer on the conductive layer from Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

20 70. The method of claim 68, further comprising forming the at least one upper metal layer as a plurality of upper metal layers.

25 71. The method of claim 68, further comprising forming the at least one upper metal layer of titanium or titanium nitride.

72. The method of claim 68, further comprising forming the at least one upper metal layer by vapor deposition.

73. The method of claim 72, wherein the vapor deposition is effected by CVD, PVD or PECVD.

74. The method of claim 55, further comprising removing the dielectric layer and portions of the at least one metal layer not underlying the aperture.

75. The method of claim 74, further comprising removing the dielectric layer by using a hydrofluoric acid wet etch solution or an oxide dry etch process.

76. The method of claim 74, further comprising removing the portions of the at least one metal layer by directional etching.

77. A method for making a metallization structure comprising:
forming a substrate comprising at least one metal layer on the surface thereof;
forming a dielectric layer over the at least one metal layer;
forming an aperture through the dielectric layer to expose a surface of the at least one metal layer;
forming a conducting layer in the aperture;
forming at least one upper metal layer overlying the dielectric layer and the conducting layer in the aperture;
removing portions of the at least one upper metal layer overlying the dielectric layer, removing the dielectric layer, and removing portions of the at least one metal layer surrounding the conducting layer to form a multi-layer metal structure having at least one sidewall; and
forming a metal spacer on the at least one sidewall of the multi-layer metal structure.

78. The method of claim 77, further comprising forming the dielectric layer of silicon oxide.

79. The method of claim 77, further including forming the at least one metal layer of Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

5 80. The method of claim 79, wherein the at least one metal layer comprises a first metal layer, and further including forming a second metal layer between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

10 81. The method of claim 77, further including forming the at least one metal layer of titanium or titanium nitride.

82. The method of claim 77, further comprising forming the at least one metal layer by vapor deposition.

15 83. The method of claim 82, further comprising forming the at least one metal layer by CVD, PVD or PECVD.

84. The method of claim 77, further comprising forming the conducting layer by vapor deposition.

20 85. The method of claim 84, further comprising forming the conducting layer by CVD, PVD or PECVD.

86. The method of claim 77, further comprising forming the at least one metal layer and the metal spacer of the same metal.

25 87. The method of claim 77, further comprising forming the metal spacer by vapor deposition of a metal layer over the multi-layer metal structure and directional etching of the vapor-deposited metal layer.

88. The method of claim 77, further including forming the metal spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN or TiN.

5 89. The method of claim 88, further including forming the metal spacer of titanium or titanium nitride.

10 90. The method of claim 77, further comprising forming the at least one upper metal layer on the conducting layer from Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

91. The method of claim 90, further comprising forming the at least one upper metal layer as a plurality of upper metal layers.

15 92. The method of claim 77, further comprising forming the at least one upper metal layer of titanium or titanium nitride.

93. The method of claim 77, further comprising forming the at least one upper metal layer by vapor deposition.

20 94. The method of claim 93, wherein the vapor deposition is effected by CVD, PVD or PECVD.

25 95. The method of claim 77, further comprising removing the dielectric layer by using a hydrofluoric acid wet etch solution or an oxide dry etch process.

96. The method of claim 77, further comprising removing the portions of the at least one metal layer by directional etching.

97. The method of claim 77, further comprising forming the conducting layer from at least one of aluminum and copper.

98. The method of claim 77, comprising forming ^{at least one} the metal layer, metal spacer, and ^{the at least one} upper metal layer of the same metal.

99. The method of claim 98, wherein the metal is Ti.

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